Receipt 4/CFR
Lewis
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rajendran Nair et al.

Title: DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION

Docket No.: 884.229US1
Filed: December 14, 1999
Examiner: Unknown

Serial No.: 09/460,742
Due Date: N/A
Group Art Unit: 2815

Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the attached:

X Communication Re: Incorrect Filing Receipt (1 pg.)

X Copy of Filing Receipt (1 pg.)

X A return postcard.

X Copy of the first page of the application (1 pg.)

No Additional fee is required.

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described above, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 22nd day of February, 2000.

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COMMUNICATION RE: INCORRECT FILING RECEIPT

Assistant Commissioner for Patents
Washington, D.C. 20231

Applicants hereby request correction of the Filing Receipt with respect to the above-identified patent application. In the Filing Receipt received February 3, 2000, (copy enclosed), the Title is incorrect and should be corrected to reflect, *DEVICE AND METHOD FOR CONTROLLING VOLTAGE **VARIATION*** as evidenced by the first page of the application as filed December 14, 1999 (copy enclosed).

Applicants would appreciate the above-identified printing error be corrected and that a new "corrected" filing receipt be sent to Applicants' representatives at the address given below.

Respectfully submitted,

RAJENDRAN NAIR ET AL.

By their Representatives,

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Date February 3, 2000 By Danny J. Padys

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant commissioner for Patents, Washington, D.C. 20231,
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Jason And

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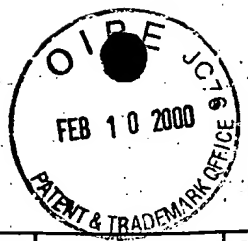

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/460,742	12/14/99	2815	$1,450.00	884.229US1	6	28	10

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MINNEAPOLIS MN 55402

DV SEP. 14, 2000 - 9 months
OCT. 29, 2000 - 10½ months
DEC. 14, 2000 - CONV. EXT

COPY

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts of Application" ("Missing Parts Notice") in this application, please submit any corrections to this Filing Receipt with your reply to the "Missing Parts Notice." When the PTO processes the reply to the "Missing Parts Notice," the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s) RAJENDRAN NAIR, HILLSBORO, OR; VIVEK K. DE, BEAVERTON, OR.

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 01/27/00
TITLE
DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARILATION

PRELIMINARY CLASS: 257

DATA ENTRY BY: SASFAI, DAVID J. TEAM: 03 DATE: 01/27/00

(See reverse for new important information)

DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION

Field of the Invention

This invention relates to controlling voltage variations, and more particularly to using voltage variable capacitors to control voltage variations in electronic systems.

Background of the Invention

As synchronous digital systems are operated at lower voltages, multiple voltages, and higher frequencies, and as the number of logic cells that make up the systems increase, new problems arise in supplying power to the systems. Some of the problems include decoupling multiple voltage power supplies, damping power supply grid network resonances, and decoupling noise in power supply signals operating at low voltages.

For digital systems fabricated using mixed technologies and multiple voltages on a single substrate, the acceptable variation in the voltages are becoming more complex. For example, a system specification may define acceptable variations that are asymmetrical in the voltages. In a system requiring a 1.8 volt power supply and a 1.0 volt power supply, the 1.0 volt power supply may be required to maintain a value above 1.02 volts while the 1.8 volt supply may be permitted to rise to 2.0 volts. Digital systems having such specifications are typically decoupled by connecting a number of individual capacitive elements to each power supply voltage line near the logic cells being powered. Unfortunately, fabricating a number of separate capacitive elements for each cell and for each power supply line is very expensive in terms of space on the surface of the substrate.

Synchronous digital systems, such as microprocessors, packaged using controlled collapse chip connection technology can have hundreds of power connection points coupled to hundreds of thousands of digital cells decoupled by hundreds of thousands of fixed capacitors. The circuit formed by the power supply, the power lines, the parasitic inductances and capacitors, the power connection points, the digital cells, and the fixed capacitors form a power connection grid network. For large transient current events that occur in synchronous digital systems, the network can experience resonant oscillations. During the development of synchronous digital systems, simulations of the logic circuits